



PATENT  
8031-1028

1FW  
\$

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of: Yoshihiro NONAKA

Appl. No.: 10/648,256

Conf.: 5218

Filed: August 27, 2003

Group: 2811

Examiner: Ori Nadav

Title: SEMICONDUCTOR INTEGRATED CIRCUIT, METHOD OF  
MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT,  
CHARGE PUMP CIRCUIT, LAYOUT DESIGNING APPARATUS,  
AND LAYOUT DESIGNING PROGRAM

PETITION FOR EXTENSION OF TIME

Assistant Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

March 11, 2005

Sir:

The undersigned hereby petitions for an extension of  
time to respond to the Official Action of January 11, 2005 for  
one month to March 11, 2005

Please charge the extension fee of \$120 to Deposit  
Account No. 25-0120. If this fee is insufficient, the Patent  
Office is hereby authorized to charge any additional extension  
fee to Deposit Account No. 25-0120. A duplicate copy of this  
sheet is enclosed.

A responsive paper is filed herewith.

Respectfully submitted,

YOUNG & THOMPSON

03/15/2005 MBYENE1 00000032 250120 10648256

01 FC:1251 120.00 DA

Robert J. Patch, Reg. No. 17,355  
745 South 23<sup>rd</sup> Street  
Arlington, VA 22202  
Telephone (703) 521-2297  
Telefax (703) 685-0573  
(703) 979-4709

RJP/mjr  
March 11, 2005